PONTIFICIA UNIVERSIDAD CATÓLICA DE CHILE
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING
ABET COURSE SYLLABI

IEE2783 DIGITAL SYSTEMS LABORATORY

Credits and contact hours:	5 UC credits / 5 hours a week labs
Instructor's name:	Enrique Álvarez
Course coordinator's name	To be defined
Textbook:	Verilog Digital System Design: Register Transfer Level Synthesis, Testbench, and Verification. McGraw Hill, 2005.
Course Catalog Description:	This course allows the student to review the contents studied during the undergraduate course of digital systems through the implementation in FPGA of complex digital systems.
Prerequisite Courses:	IEE2713 Digital Systems, IEE2183 Electrical Measurements Laboratory
Co-requisite Courses:	To be defined
Status in the Curriculum:	Elective
Course Learning Outcomes:	1. Design and implementation of complex digital systems using discrete components (TTL and HC) and mainly FPGAs. 2. Learn hardware-oriented programing languages such as Verilog. 3. Solve engineering problems with given specifications by developing digital systems.
Relation of Course to ABET Criteria:	a. Knowledge of mathematics, science and engineering b. Design and conduct experiments: analyze and interpret data c. Design a system, component, or process d. Multidisciplinary teams e. Identify, formulate, and solve engineering problems i. Recognition of the need for, and an ability to engage in life-long learning k. Techniques, skills, and modern tools for engineering practice.

Topics covered:

1. Experience 1 – TTL, HC and FSM design
   a. Characterization of TTL and HC technologies
   b. Design and discrete implementation of an FSM for and specific engineering problem
2. Experience 2 - EEPROM
   a. Design and implementation of an asynchronous serial communication protocol using an EEPROM for combinational logic
3. Experience 3 – Introduction to the FPGA
   a. Design and implementation of a function generator using an FPGA
4. Experience 4 – Pong
   a. Use of peripherals such as the VGA
   b. Design and implementation in FPGA of the game Pong
5. Experience 5 – Digital Piano
   a. Use of peripherals such as a computer keyboard (PS2 protocol)
   b. Design and implementation in FPGA of a two-octaves piano.
6. Project
   a. Design and implementation in FPGA of a complex digital system