PONTIFICIA UNIVERSIDAD CATÓLICA DE CHILE
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING
ABET COURSE SYLLABI

IEE2713 DIGITAL SYSTEMS

Credits and contact hours:	10 UC credits / 10 hours (3 h. Lectures ; 1.5 h. Problems sessions and 5.5 h. Independent learning experiences)
Instructor's name:	Marcelo Guarini (Semester I) and Cristián Tejos (Semester II)
Course coordinator's name	To be defined
Textbook:	S. Brown, Z. Vranesic, "Fundamentals of Digital Logic with Verilog Design", Mc Graw Hill, 2003. D. M. Harris & S. L. Harris, "Digital Design and Computer Architecture", 2nd edition, Elsevier, 2013.
Course Catalog Description:	The aim of this course is to enable students to analyze and design simple and advanced digital systems and circuits, using digital integrated systems and programmable logic devices.
Prerequisite Courses:	MAT1203 Linear Algebra
Co-requisite Courses:	To be defined
Status in the Curriculum:	Elective
Course Learning Outcomes:	1. To analyze and design combinational digital systems using Boolean algebra and Karnaugh maps. 2. To analyze and design sequential digital systems using Karnaugh maps and finite state machines. 3. To simulate, test and program combinational and sequential digital systems using hardware description languages (Verilog).
Relation of Course to ABET Criteria:	a. Knowledge of mathematics, science and engineering b. Design and conduct experiments: analyze and interpret data c. Design a system, component, or process e. Identify, formulate, and solve engineering problems j. Knowledge of contemporary issues k. Techniques, skills, and modern tools for engineering practice.
Topics covered:	1. Introduction 1.1. Numerical systems. 1.2. Logic gates and their parameters. 1.3. MOS transistors. 2. Design of combinational logic systems

2.1. Boolean algebra Boolean.
2.2. Implementation of Boolean functions.
2.3. Multi-level combinational logic.
2.4. Karnaugh maps.
2.5. Combinational blocks and temporal behavior.

3. Design of sequential logic systems
   3.1. Latches y flip-flops.
   3.2. Design of synchronous logic systems.
   3.3. Finite state machines.
   3.4. Timing of sequential logic.
   3.5. Parallelism.
4. Hardware description Language
   4.1. Combinational logic.
   4.2. Structural modeling.
   4.3. Sequential logic.
   4.4. Finite state machines.
   4.5. Parameterized modules.
   4.6. Test benches.
5. Digital building blocks
   5.1. Arithmetic circuits.
   5.2. Number systems.
   5.3. Sequential building blocks.
   5.4. Memory arrays.
   5.5. Logic arrays.
6. Architecture
   6.1. Assembler language.
   6.2. Machine language.
   6.3. Programming.
   6.4. Addressing modes.
7. Microarchitecture
   7.1. Single-cycle processor
   7.2. Multi-cycle processor
   7.3. Pipelined processor.